CLAIMS

What is claimed is:

1.   An application specific integrated circuit (ASIC) comprising:

a standard cell, the standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable (FP) function coupled to the at least one bus and at least a portion

of the plurality of internal signals, wherein the FP function provides access to internal signals

for observation and control.

2.   The ASIC of claim 1 wherein the FP function comprises a signal connector

function.

3.   The ASIC of claim 2 wherein the signal connector function comprises a first

logic for providing an external I/O function and a second logic which is in communication with

the first logic that selects the appropriate internal signals for external observation and control.

4.   The ASIC of claim 1 wherein the FP function includes a testing function.

5.   The ASIC of claim 4 wherein the testing function includes a selector function

for selecting the signals of interest and a validation function coupled to the selector function for

testing the signals of interest.

1   6.   The ASIC of claim 5 wherein the testing function includes a test program for

2   validating at least one of the plurality of logic functions.

1   7.   The ASIC of claim 1 wherein the FP function includes an error recovery

2   function.

1   8.   The ASIC of claim 7 wherein the error recovery function comprises

2   determining if an error is observed, determining the error case when an error is observed and

3   corrected.

1   9.   The ASIC of claim 8 wherein the error recovery function further includes

2   writing an error code to an external system based upon the error case.

1   10.   The ASIC of claim 8 wherein the error recovery function utilizes a watchdog

2   function.

1   11.   The ASIC of claim 9 wherein the watchdog function comprises determining

2   after a predetermined time-period or number of actions if a portion of the ASIC is operating

3   properly, and invoking an error-handling process if the portion is not operating properly.

1   12.   The ASIC of claim 1 wherein the FP function comprises a field programmable

2   gate array function.

1   13.   A method for providing a testing function in an application specific integrated

2   circuit (ASIC), the ASIC including a standard cell, the standard cell including a plurality of

3   logic functions, the method comprising the steps of:

4   (a)   providing a field programmable (FP) function in the ASIC; and

5   (b)   providing a test program in the FP function.

1   14.   The method of claim 13 wherein the test program validates at least one of the

2   plurality of logic functions.

1   15.   A method for allowing an application specific integrated circuit to operate after

2   an error has occurred therein, the method comprising the steps of:

3   (a)   providing a field programmable (FP) function in the ASIC; and

4   (b)   providing an error recovery function within the FP function.

1   16.   The ASIC of claim 15 wherein the error recovery function comprises

2   determining if an error is observed, determining the error case when an error is observed and

3   corrected.

1   17.   The ASIC of claim 16 wherein the error recovery function further includes

2   writing an error code to an external system based upon the error case.

1   18.   The ASIC of claim 16 wherein the error recovery function utilizes a watchdog

2   function.

1   19.   The ASIC of claim 18 wherein the watchdog function comprises determining

2   after a predetermined time-period or number of actions if a portion of the ASIC is operating

3   properly, and invoking an error-handling process if the portion is not operating properly.